WAGO I/O SYSTEM 750

Fieldbus Independent I/O Modules

Counter Modules 750-404, (/xxx-xxx)

Manual

Version 1.1.2

WAGO® INNOVATIVE CONNECTIONS

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Every conceivable measure has been taken to ensure the correctness and completeness of this documentation. However, as errors can never be fully excluded, we would appreciate any information or ideas at any time.

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We wish to point out that the software and hardware terms as well as the trademarks of companies used and/or mentioned in the present manual are generally trademark or patent protected.

Content

1 Important Comments

To ensure fast installation and start-up of the units described in this manual, we strongly recommend that the following information and explanations are carefully read and abided by.

1.1 Legal Principles

1.1.1 Copyright

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1.1.2 Personnel Qualification

The use of the product detailed in this manual is exclusively geared to specialists having qualifications in PLC programming, electrical specialists or persons instructed by electrical specialists who are also familiar with the valid standards. WAGO Kontakttechnik GmbH & Co. KG declines all liability resulting from improper action and damage to WAGO products and third party products due to non-observance of the information contained in this manual.

1.1.3 Intended Use

For each individual application, the components supplied are to work with a dedicated hardware and software configuration. Modifications are only permitted within the framework of the possibilities documented in the manuals. All other changes to the hardware and/or software and the non-conforming use of the components entail the exclusion of liability on part of WAGO Kontakttechnik GmbH & Co. KG.

Please direct any requirements pertaining to a modified and/or new hardware or software configuration directly to WAGO Kontakttechnik GmbH & Co. KG.

1.2 Symbols

Danger
Always abide by this information to protect persons from injury.

Warning
Always abide by this information to prevent damage to the device.

Attention
Marginal conditions must always be observed to ensure smooth operation.

ESD (Electrostatic Discharge)
Warning of damage to the components by electrostatic discharge. Observe the precautionary measure for handling components at risk.

Note
Routines or advice for efficient use of the device and software optimization.

More information
References on additional literature, manuals, data sheets and internet pages.

1.3 Number Notation

Number Code	Example	Note
Decimal	100	normal notation
Hexadecimal	0x64	C notation
Binary	'100' '0110.0100'	within inverted commas, nibble separated with dots

1.4 Safety Notes

Warning
Switch off the system prior to working on bus modules!

In the event of deformed contacts, the module in question is to be replaced, as its functionality can no longer be ensured on a long-term basis.

The components are not resistant against materials having seeping and insulating properties. Belonging to this group of materials is: e.g. aerosols, silicones, triglycerides (found in some hand creams).

If it cannot be ruled out that these materials appear in the component environment, then additional measures are to be taken:
- installation of the components into an appropriate enclosure
- handling of the components only with clean tools and materials.

Attention
Cleaning of soiled contacts may only be done with ethyl alcohol and leather cloths. Thereby, the ESD information is to be regarded.

Do not use any contact spray. The spray may impair the functioning of the contact area.

The WAGO-I/O-SYSTEM 750 and its components are an open system. It must only be assembled in housings, cabinets or in electrical operation rooms. Access must only be given via a key or tool to authorized qualified personnel.

The relevant valid and applicable standards and guidelines concerning the installation of switch boxes are to be observed.

ESD (Electrostatic Discharge)
The modules are equipped with electronic components that may be destroyed by electrostatic discharge. When handling the modules, ensure that the environment (persons, workplace and packing) is well grounded. Avoid touching conductive components, e.g. gold contacts.

1.5 Scope

This manual describes the Special Module 750-404, (/xxx-xxx) Counter Modules of the modular WAGO-I/O-SYSTEM 750.

Handling, assembly and start-up are described in the manual of the Fieldbus Coupler/Controller. Therefore this documentation is valid only in the connection with the appropriate manual.

2 I/O Modules

2.1 Specialty Modules

2.1.1 Overview Counter Modules 750-404, (/xxx-xxx)

I/O Module	750-404	750-404/ 000-001	750-404/ 000-002	750-404/ 000-003	750-404/ 000-004	750-404/ 000-005
Function	Up / Down Counter	Up Counter / Enable Input	Peak Time Counter	Frequency Counter	Up / Down Counter / Switch Output	2 Up Counter
Channels	1	1	1	1	1	2
Switching rate	max. 100 kHz	max. 100 kHz	max. 10 kHz	0,1 Hz ... 100 kHz	max. 100 kHz	max. 5 kHz
Counter depth	32 bit	32 bit	32 bit	32 bit	32 bit	16 bit

2.1.2 750-404 [Up/Down Counter /100 kHz]

Up/Down Counter, DC 24 V, 100 kHz

2.1.2.1 Variations

Item-No.	Designation	Description
750-404	Up/Down Counter / 100 kHz	Up/Down Counter, DC 24 V, 100 kHz
750-404/000-002	Peak Time Counter	Peak Time Counter, DC 24 V, 10 kHz
750-404/000-004	Up / Down Counter / Switch Output	Up/Down Counter, 24 V, 100kHz, Switch Output

2.1.2.2 View

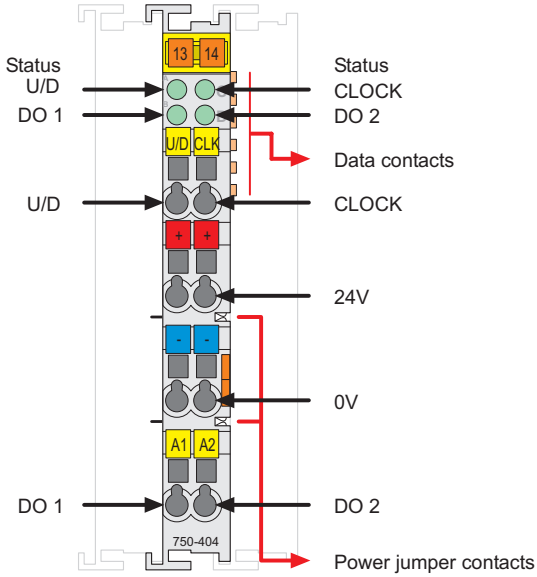

Fig. 2.1.2-1: Up/Down Counter 750-404 g040400e

2.1.2.3 Description

The Up/Down counter 750-404 and the variation 750-404/000-004 is capable of counting binary pulses of DC 24 V at the input CLOCK and then transmits the data to the fieldbus.
The counter module 750-404/000-002 begins processing with pulses at the CLOCK input and counts the pulses in a special time span. The time span is given as 10 s.

The changes from 0 V to 24 V are counted

The counter counts up, if the input U/D is set at 24 V. With an open circuit input or 0 V the counter counts backwards.

The counter can be set or reset with the control byte.

The digital outputs DO 1 and DO 2 of the counter module 750-404 and the variation 750-404/000-002 are activated through bits in the control byte. The digital outputs DO 1 and DO 2 of the counter module 750-404/000-004 are activated depending on the counter reading or through bits in the control byte.

The outputs are short-circuit-protected.

The high states of the inputs U/D and CLOCK and the digital output channels are each indicated by a green LED.

An optocoupler is used for electrical isolation between the bus and the field side.

Any configuration of the counter modules is possible when designing the fieldbus node. Grouping of module types is not necessary.

The field side supply voltage of 24 V for the counter module is derived from adjacent I/O modules or from a supply module. The supply voltage for the field side is made automatically through the individual I/O modules by means of power jumper contacts.

Warning
The maximum current of the internal power jumper contacts is 10 A. When configuring the system it is important not to exceed the maximum/sum current. However, if such a case should occur, another supply module must be added.

Attention
This module has no power contacts for receiving and transmitting the ground (earth) potential. A supply module is required, if the adjacent modules need to be connected to the ground.

Note
Use an appropriate supply module (e.g. 750-602) if an electrically isolated voltage supply is required!

The module 750-404 and the variations 750-404/000-002 and 750-404/000-004 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, 750-323, 750-324 and 750-327 and the ModBus controllers 750-812, 750-812/025-000 and 750-814).

2.1.2.4 Display Elements

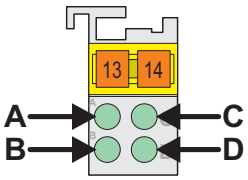

Fig. 2.1.2-2: Display Elements g041402x

LED	Channel	Meaning	State
A green	Status U/D	off	Input U/D: Signal voltage (0), Backwards counting
		on	Input U/D: Signal voltage (1), Forward counting
B green	Status CLOCK	off	Input CLOCK: Signal voltage (0)
		on	Input CLOCK: Signal voltage (1) Counting pulse
C green	Status DO 1	off	Digital Output DO 1 reset
		on	Digital Output DO 1 setting
D green	Status DO 2	off	Digital Output DO 2 reset
		on	Digital Output DO 2 setting

2.1.2.5 Schematic Diagram

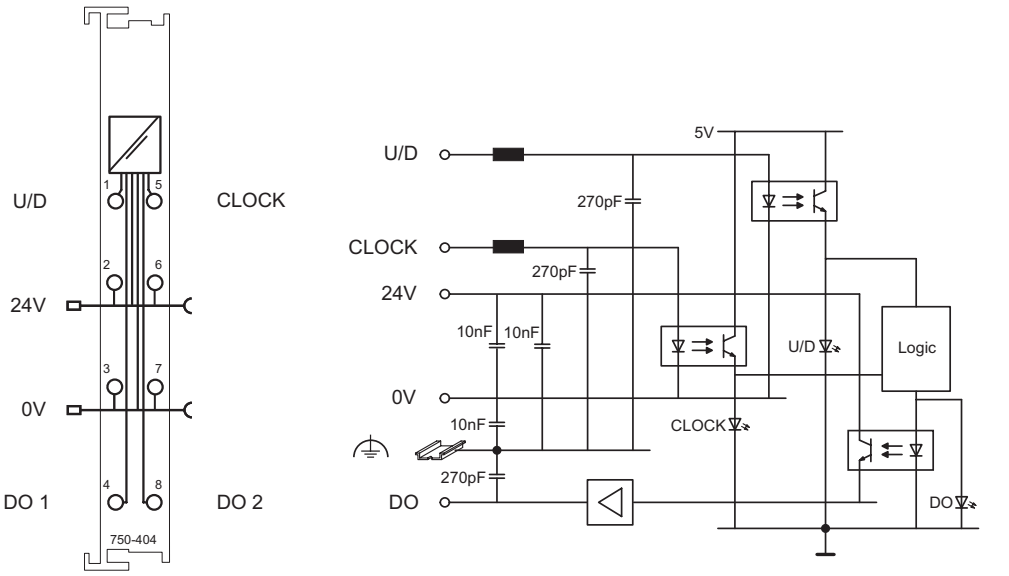

Fig. 2.1.2-3: Up/Down Counter 750-404 g040401e

2.1.2.6 Technical Data

Module Specific Data		
Number of outputs	2	
Number of counters	1	
Output current	0.5 A short-circuit-protected	
Current consumption (internal)	15 mA	
Voltage via power jumper contacts	DC 24 V (-15 % ... + 20 %)	
Signal voltage	(0): DC –3 V ... +5 V (1): DC +15 V ... +30 V	
Switching rate $_{max.}$	100 kHz (750-404, 750-404/000-004) 10 kHz (750-404/000-002)	
Input current $_{typ.}$	6 mA	
Counter depth	32 bits data	
Isolation	500 V (System/Supply)	
Internal bit width	32 bits data 8 bits control /status	
Dimensions (mm) W x H x L	12 x 64* x 100 * from upper edge of 35 DIN rail	
Weight	ca. 55 g	
Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)		
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)	
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)	
Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	$_{C}UL_{US}$ (UL508)	
	ABS (American Bureau of Shipping)	
	BV (Bureau Veritas) (applied for)	
	DNV (Det Norske Veritas)	Cl. B
	GL (Germanischer Lloyd) (applied for)	Cat. A, B, C, D
	KR (Korean Register of Shipping)	
	LR (Lloyd's Register)	Env. 1, 2, 3, 4
	NKK (Nippon Kaiji Kyokai)	
	$_{C}UL_{US}$ (UL1604)	Class I Div2 ABCD T4A
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	

More Information
Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which you can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412)
or in the internet under:
www.wago.com → Documentation → WAGO-I/O-SYSTEM 750 → System Description

2.1.2.7 Process Image

Using the I/O module 750-404, a 5 byte input and output process image can be transferred to the fieldbus coupler / controller via one logical channel.

The transfer of the setting counter value in binary format is made via 4 output bytes (D0 ... D3) and the transfer of the counter reading in binary format is made via 4 input bytes (D0 ... D3). The control byte C0 serves for setting the counter and the outputs. The status byte S0 shows the status of the counter and the inputs and outputs.

Attention
The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte 0	C0	Control byte 0
D0	Counter value byte 0 (LSB)	D0	Set value byte 0 (LSB)
D1	Counter value byte 1	D1	Set value byte 1
D2	Counter value byte 2	D2	Set value byte 2
D3	Counter value byte 3 (MSB)	D3	Set value byte 3 (MSB)

2.1.2.7.1 Control- / Status byte 750-404

The control byte C0 serves for setting and locking the counter and for setting the outputs. The status byte S0 shows the status of the counter and the inputs and outputs.

Control byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	Set counter	Lock counter	Set output DO 2	Set output DO 1	0	0

0 This constant must be set to zero.

Status byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	Counter is set	Counter is blocked	actual signal at output DO 2	actual signal at output DO 1	actual signal at input U/D	actual signal at input CLOCK

X This value is not evaluated.

With the control and status byte the following tasks are possible:

Set Counter:
Put Bit 5 into the control byte. The counter with the 32 bit value is loaded into output bytes 0-3. As long as the bits are set, the counter can stop and information is stored. The ensuing data of the counter will be conveyed to the status byte.

Lock Counter:
Bit 4 is set into the control byte, then the count process is suppressed. Bit 4 in the status byte communicates the suppression of the counter.

Set/ Reset Outputs:
Bits 2 and 3 set the additional two outputs of the counter module.

2.1.2.7.2 Control- / Status byte 750-404/000-002

The control byte C0 serves for starting the periodic counter pulse measurement and for setting the outputs. The status byte S0 shows the status of the counter and the inputs and outputs.

Control byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	Start of the periodic counting	0	Set output DO 2	Set output DO 1	0	0

0 This constant must be set to zero.

Status byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	Counting starting	X	actual signal at output DO 2	actual signal at output DO 1	actual signal at input U/D	Toggelbit for end of the record

X This value is not evaluated.

The counter begins processing with pulses at the CLOCK input and counts the pulses in a special time span. The time span is given as 10 s.

The state of the counter is stored in the process image until the next period. After the recording the counting starts again at 0.

The activation of the counting and the synchronization with the SPS is made by a handshake in the control and status byte.

The end of the counting period and thus the new process data is signaled by a toggle bit in the status byte.

2.1.2.7.3 Control- / Status byte 750-404/000-004

The control byte C0 serves for setting and locking the counter and for setting the outputs dependent or independently on the counter reading. The status byte S0 shows the status of the counter and the inputs and outputs.

Control byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	Set counter	Lock Counter	Set output DO 2	Set output DO 1	Output O2 activated dependin g of the counter value	Output O1 activated dependin g of the counter value

0 This constant must be set to zero.

Status byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	Counter is set	Counter is blocked	actual signal at output DO 2	actual signal at output DO 1	actual signal at input U/D	actual signal at input CLOCK

X This value is not evaluated.

With the control and status byte the following tasks are possible:

Set Counter:
Put Bit 5 into the control byte. The counter with the 32 bit value is loaded into output bytes 0-3. As long as the bits are set, the counter can stop and information is stored. The ensuing data of the counter will be conveyed to the status byte.

Lock Counter:
Bit 4 is set into the control byte, then the count process is suppressed. Bit 4 in the status byte communicates the suppression of the counter.

Switching the outputs dependent of the counter:
The bits 0 and 1 activate the function: output dependent setting of binary outputs. If the counter reading 0x80000000 is exceeded, output DO 1 is activated. For the output DO 2 only the bottom 16 bits of the counter reading are taken into account, which means that output DO 2 is activated as soon as the counter reading 0x8000 is exceeded. Having reached 0 again, the outputs are reset.

Set Outputs:
Bits 2 and 3 set the digital outputs DO 1 and DO 2 of the counter module. If bits 2 or 3 are also set, they have priority before bits 0 and 1, so that the corresponding output is set independent of the counter reading.

2.1.2.8 Examples

2.1.2.8.1 750-404

Set Counter:
First of all the counter reading is set to 100 by "Setting counter", i. e. to the hexadecimal value: 0x64.

1. Enter the counter reading in the output data.
   The data bytes D0 to D3 of the output data then read as follows:

Data bytes				
Output data	**D3**	**D2**	**D1**	**D0**
Value	0x00	0x00	0x00	0x64

2. Validate the counter reading in the control byte with bit 5 (setting counter) to have it adopted as an output value. The control byte has the following bits:

Control byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	1	X	X	X	X	X

3. Wait for the feedback from the counter module in the status byte, bit 5 (counter set). The status byte has the following bits:

Status byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	X	X	1	X	X	X	X	X

4. Delete bit 5 (setting counter) in the control byte in order to finish the Handshake. The bits in the control byte read as follows:

Control byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	0	X	X	X	X	X

5. The set counter reading then appears in the input data with the following data bytes D0 to D3:

Data bytes				
Input bit	**D3**	**D2**	**D1**	**D0**
Wert	0x00	0x00	0x00	0x64

X is used if a value is not relevant.

Up counting:

Attention
For counting up, 24 V must be applied to input U/D.

6. Wait for the first and further count pulses.
   During counting, the data bytes D0 to D3 of the input data appear as follows:

	Data bytes			
Remark	**D3**	**D2**	**D1**	**D0**
no count pulse received	0x00	0x00	0x00	0x64
1st count pulse received	0x00	0x00	0x00	0x65
2nd count pulse received	0x00	0x00	0x00	0x66
Further count pulses	.....	.....	.....	.....
Max. counter reading reached	0xFF	0xFF	0xFF	0xFF
the next count pulse causes a number overflow	0x00	0x00	0x00	0x00
One further count pulse received	0x00	0x00	0x00	0x01

2.1.2.8.2 750-404/000-002

1. The counter counts up (the input U/D is set at 24 V). The counter reading is 0. The timer interrupts. No count pulse received on the input CLOCK.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	0	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	0	0	X	X	1	0

2. The cyclic period measurement is requested. The counter reading is 0. The timer interrupts. No count pulse received on the input CLOCK.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	0	0	X	X	1	0

3. The cyclic period measurement is started. The counter reading is 0. The timer runs with the parameterized cycle time. Count pulses received on the input CLOCK.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	1	0

4. The cyclic period measurement is running. The counter reading is reset and the timer is started again. The process data supply the number of impulses, which were registered in the previous cycle.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	1	1

5. The cyclic period measurement is running. The counter reading is reset and the timer is started again. The process data supply the number of impulses, which were registered in the previous cycle.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	1	0

6. The cyclic period measurement is running. Stopping the cyclic recording was requested. The process data supply the counter reading, which was registered in the previous cycle.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	0	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	1	0	X	X	1	X

7. The cyclic period measurement is stopped. The counter reading is reset. The process data supply the value 0.

Control byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	0	0	X	X	0	0

Status byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	0	0	0	X	X	1	0

2.1.2.8.3 750-404/000-004

Set the digital output DO 1 after 4.000 pulses have been counted. There are several possibilities to set an output.

If DO 1 is used as an automatic switching output and if the counter is to count up, set the counter to
0x80000000 - 4000 = 0x7FFFF060
and apply + 24V to the U/D input. Furthermore, activate bit 0 in the control byte. After 4000 pulses, the counter reading of 0x80000000 is reached and output DO 1 activated.

If you wish the counter to count down, pre-set
0x80000000 + 4000 = 0x80000FA0
and apply 0V to U/D. After 4000 pulses the counter reading 0x80000000 is reached and output DO 1 deactivated.

If DO 2 is to be used as a switching output, load the counter with
0x8000 - 4000 = 0x7060 or
0x8000 + 4000 = 0x8FA0
respectively, because only the bottom 16 bits of the counter are used for switching output DO 2. Instead of bit 0 now activate bit 1 in the control byte.

The binary output not involved each time can be directly addressed by the controls via bit 2 and 3.

2.1.3 750-404/000-001 [Up Counter / Enable Input]

Up Counter / Enable Input, DC 24 V, 100 kHz

2.1.3.1 View

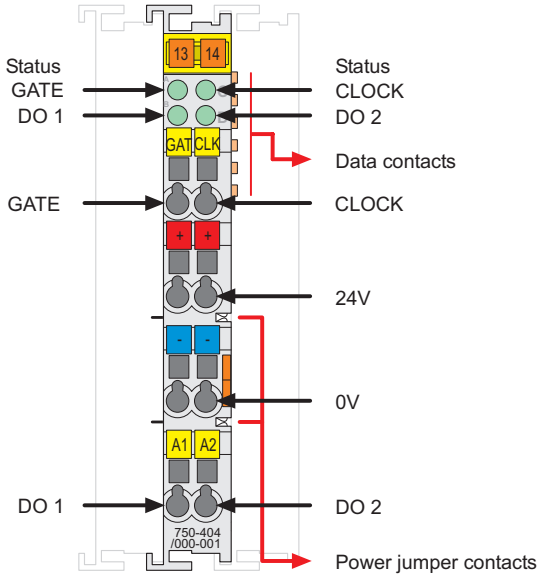

Fig. 2.1.3-1: Up Counter 750-404/000-001 g040404e

2.1.3.2 Description

The Up counter is capable of counting binary pulses of DC 24 V at the input CLOCK and then transmits the data to the fieldbus. The changes from 0 V to 24 V are counted.

The counter is locked with an open circuit or 0 V on input GATE. With +24 V on input GATE, the counter is enabled.

The counter can be set or reset with the control byte.

The digital outputs DO 1 and DO 2 are activated through bits in the control byte.

The outputs are short-circuit-protected.

The high states of the inputs GATE and CLOCK and the digital output channels are each indicated by a green LED.

An optocoupler is used for electrical isolation between the bus and the field side.

Any configuration of the counter modules is possible when designing the fieldbus node. Grouping of module types is not necessary.

The field side supply voltage of 24 V for the counter module is derived from adjacent I/O modules or from a supply module. The supply voltage for the field side is made automatically through the individual I/O modules by means of power jumper contacts.

Warning
The maximum current of the internal power jumper contacts is 10 A. When configuring the system it is important not to exceed the maximum/sum current. However, if such a case should occur, another supply module must be added.

Attention
This module has no power contacts for receiving and transmitting the ground (earth) potential. A supply module is required, if the adjacent modules need to be connected to the ground.

Note
Use an appropriate supply module (e.g. 750-602) if an electrically isolated voltage supply is required!

The module 750-404/000-001 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, 750-323, 750-324 and 750-327 and the ModBus controllers 750-812, 750-812/025-000 and 750-814).

2.1.3.3 Display Elements

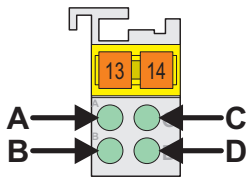

Fig. 2.1.3-2: Display Elements g041402x

LED	Channel	Meaning	State
A green	Status GATE	off	Input GATE: Signal voltage (0), Counting closed
		on	Input GATE: Signal voltage (1), Counting approved
B green	Status CLOCK	off	Input CLOCK: Signal voltage (0)
		on	Input CLOCK: Signal voltage (1)
C green	Status DO 1	off	Digital Output DO 1 reset
		on	Digital Output DO 1 setting
D green	Status DO 2	off	Digital Output DO 2 reset
		on	Digital Output DO 2 setting

2.1.3.4 Schematic Diagram

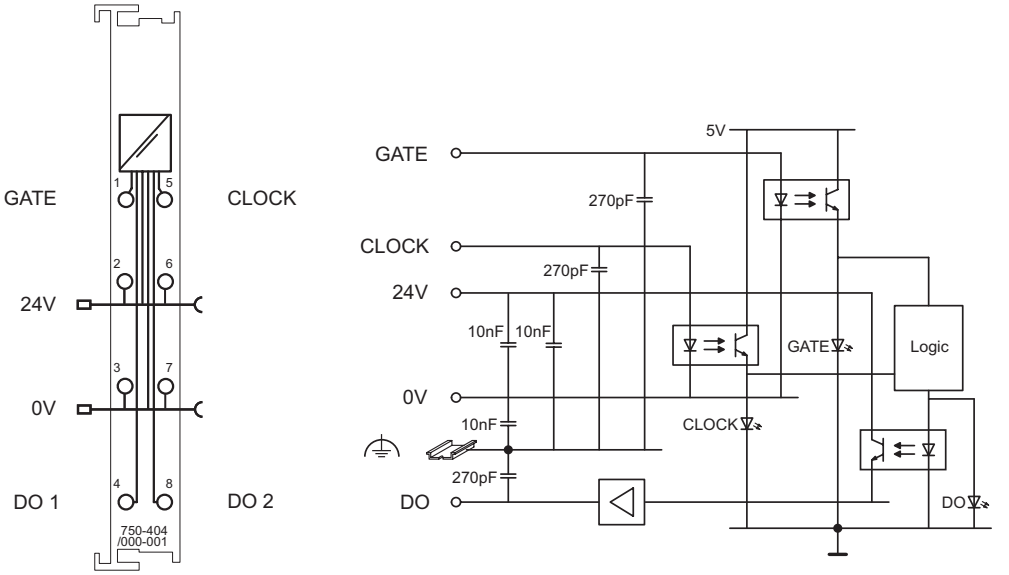

Fig. 2.1.3-3: Up Counter 750-404/000-001 g040405e

2.1.3.5 Technical Data

Module Specific Data		
Number of outputs	2	
Number of counters	1	
Output current	0.5 A short-circuit-protected	
Current consumption (internal)	15 mA	
Voltage via power jumper contacts	DC 24 V (-15 % ... + 20 %)	
Signal voltage	(0): DC –3 V ... +5 V (1): DC +15 V ... +30 V	
Switching rate $_{max.}$	100 kHz	
Input current $_{typ.}$	6 mA	
Counter depth	32 bits data	
Isolation	500 V (System/Supply)	
Internal bit width	32 bits data 8 bits control /status	
Dimensions (mm) W x H x L	12 x 64* x 100 * from upper edge of 35 DIN rail	
Weight	ca. 55 g	
Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)		
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)	
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)	
Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	$_{C}UL_{US}$ (UL508)	
	$_{C}UL_{US}$ (UL1604)	Class I Div2 ABCD T4A
	DNV (Det Norske Veritas)	Cl. B
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	

More Information
Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which You can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412-0001-0101) or in the Internet under:
www.wago.com -> Service /Downloads /Documentation /WAGO-I/O-SYSTEM 750/System Description/.

2.1.3.6 Process Image

Using the I/O module 750-404/000-001, a 5 byte input and output process image can be transferred to the fieldbus coupler / controller via two logical channels.

The transfer of the setting counter value in binary format is made via 4 output bytes (D0 ... D3) and the transfer of the counter reading in binary format is made via 4 input bytes (D0 ... D3). The control byte C0 serves for setting and locking the counter and for setting the outputs. The status byte S0 shows the status of the counter and the inputs and outputs.

Attention
The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte 0	C0	Control byte 0
D0	Counter value byte 0 (LSB)	D0	Set value byte 0 (LSB)
D1	Counter value byte 1	D1	Set value byte 1
D2	Counter value byte 2	D2	Set value byte 2
D3	Counter value byte 3 (MSB)	D3	Set value byte 3 (MSB)

Control byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	Set counter	Lock counter	Set output DO 2	Set output DO 1	0	0

0 This constant must be set to zero.

Status byte 0							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	Counter is set	Counter is blocked	actual signal at output DO 2	actual signal at output DO 1	actual signal at input U/D	actual signal at input CLOCK

X This value is not evaluated.

With the control and status byte the following tasks are possible:

Set Counter:
Put Bit 5 into the control byte. The counter with the 32 bit value is loaded into output bytes 0-3. As long as the bits are set, the counter can stop and information is stored. The ensuing data of the counter will be conveyed to the status byte.

Lock Counter:
Bit 4 is set into the control byte, then the count process is suppressed. Bit 4 in the status byte communicates the suppression of the counter.

Set Outputs:
Bits 2 and 3 set the additional two outputs of the counter module.

2.1.3.7 Example

Set Counter:
First of all the counter reading is set to 100 by "Setting counter", i. e. to the hexadecimal value: 0x64.

8. Enter the set value in the output data.
   The data bytes D0 to D3 of the output data then read as follows:

Data bytes				
Output data	**D3**	**D2**	**D1**	**D0**
Value	0x00	0x00	0x00	0x64

9. Validate the counter reading in the control byte with bit 5 (setting counter) to have it adopted as an output value. The control byte has the following bits:

Control byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	1	X	X	X	X	X

10. Wait for the feedback from the counter module in the status byte, bit 5 (counter set). The status byte has the following bits:

Status byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	X	X	1	X	X	X	X	X

11. Delete bit 5 (setting counter) in the control byte in order to finish the Handshake. The bits in the control byte read as follows:

Control byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	0	X	X	X	X	X

12. The set counter reading then appears in the input data with the following data bytes D0 to D3:

Data bytes				
Input bit	**D3**	**D2**	**D1**	**D0**
Value	0x00	0x00	0x00	0x64

X is used if a value is not relevant.

Up counting:

Attention
For counting up, 24 V must be applied to input GATE.

13. Wait for the first and further count pulses.
During counting, the data bytes D0 to D3 of the input data appear as follows:

Data bytes				
Remark	**D3**	**D2**	**D1**	**D0**
no count pulse received	0x00	0x00	0x00	0x64
1st count pulse received	0x00	0x00	0x00	0x65
2nd count pulse received	0x00	0x00	0x00	0x66
Further count pulses	.....	.....	.....	.....
Max. counter reading reached	0xFF	0xFF	0xFF	0xFF
the next count pulse causes a number overflow	0x00	0x00	0x00	0x00
One further count pulse received	0x00	0x00	0x00	0x01

2.1.4 750-404/000-003 [Frequency Counter 0.1 Hz-100 kHz]

Frequency Counter 0.1 Hz ... 100 kHz, DC 24 V

2.1.4.1 View

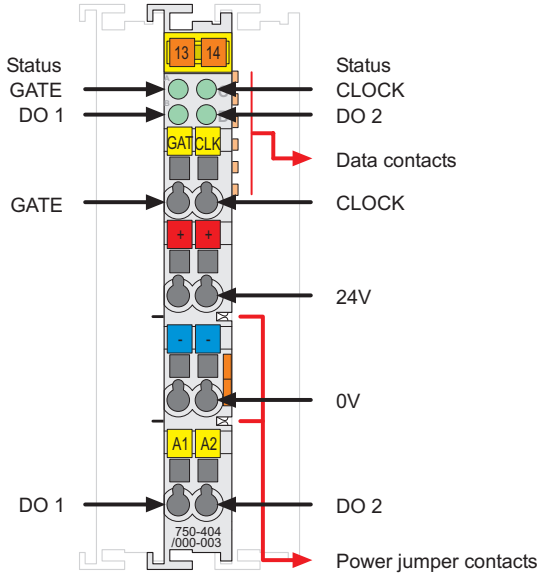

Fig. 2.1.4-1: Frequency Counter 750-404/000-003 g040408e

2.1.4.2 Description

The counter module also can be ordered as frequency counter module with 750-404/000-003.

The counter module 750-404/000-003 measures the period of the 24 V DC input signal at the input CLOCK and converts it into a corresponding frequency value. The measurement is enabled if the input GATE is an open circuit input or 0V. To disable processing, the GATE input is to be set to 24 V DC.

To recognize low frequency or near zero frequency signals, the maximum time between two data updates is parameterizable.

The digital outputs DO1 and DO2 can be activated via specific bits in the Control byte.

The outputs are short-circuit-protected.

The high states of the inputs GATE and CLOCK and the output channels are each indicated by a LED.

An optocoupler is used for electrical isolation between the bus and the field side.

Any configuration of the counter modules is possible when designing the fieldbus node. Grouping of module types is not necessary.

The field side supply voltage of 24 V for the counter module is derived from adjacent I/O modules or from a supply module. The supply voltage for the field side is made automatically through the individual I/O modules by means of power jumper contacts.

Warning
The maximum current of the internal power jumper contacts is 10 A. When configuring the system it is important not to exceed the maximum/sum current. However, if such a case should occur, another supply module must be added.

Attention
This module has no power contacts for receiving and transmitting the ground (earth) potential. A supply module is required, if the adjacent modules need to be connected to the ground.

Note
Use an appropriate supply module (e.g. 750-602) if an electrically isolated voltage supply is required!

The module 750-404/000-003 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, 750-323, 750-324 and 750-327 and the ModBus controllers 750-812, 750-812/025-000 and 750-814).

2.1.4.3 Display Elements

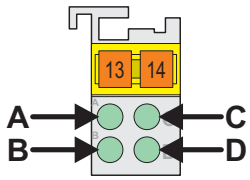

Fig. 2.1.4-2: Display Elements g041402x

LED	Channel	Meaning	State
A green	Status GATE	off	Input GATE: Signal voltage (0), Measurement released
		on	Input GATE: Signal voltage (1), Measurement disabled
B green	Status CLOCK	off	Input CLOCK: Signal voltage (0)
		on	Input CLOCK: Signal voltage (1), Counting pulse
C green	Status DO 1	off	Digital Output DO 1 reset
		on	Digital Output DO 1 setting
D green	Status DO 2	off	Digital Output DO 2 reset
		on	Digital Output DO 2 setting

2.1.4.4 Schematic Diagram

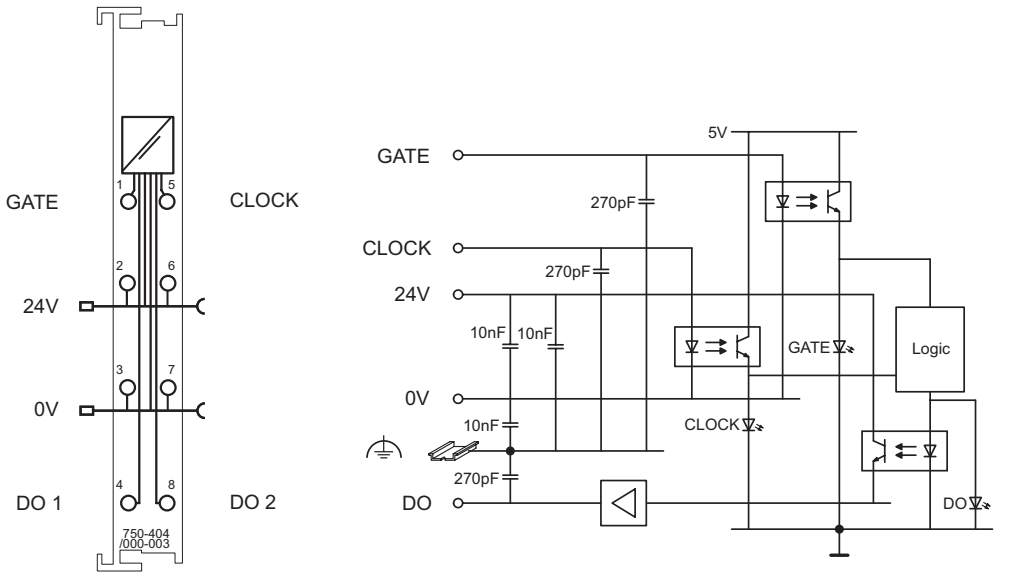

Fig. 2.1.4-3: Frequency Counter 750-404/000-003 g040409e

2.1.4.5 Technical Data

Module Specific Data	
Number of outputs	2
Number of counters	1
Output current	0.5 A short-circuit-protected
Current consumption $_{max.}$	75 mA at DC 5 V
Voltage via power jumper contacts	DC 24 V (-15 % ... + 20 %)
Signal voltage	(0): DC –3 V ... +5 V (1): DC +15 V ... +30 V
Switching rate $_{max.}$	100 kHz
Pulse width $_{min.}$	10 µs
Input current $_{typ.}$	5 mA
Counter depth	32 Bit
Isolation	500 V (System/Supply)
Internal bit width	32 bits data 8 bits control /status
Dimensions (mm) W x H x L	12 x 64* x 100 * from upper edge of 35 DIN rail
Weight	ca. 55 g
Maximum frequency range	
Integration time = 1 period	0.1 Hz - 8 kHz, resolution 0.001 Hz
Integration time = 4 period	0.25 Hz - 32 kHz, resolution 0.01 Hz
Integration time = 16 period	1 Hz - 100 kHz, resolution 0.1 Hz (1 Hz)
Measuring error at the maximum frequency range	
Range 0.1 Hz - 8 kHz	< ± 1 %
Range 0.25 Hz - 32 kHz	< ± 1.5 %
Range 1 Hz - 100 kHz	< ± 1.5 %
Lower frequency range*	
Integration time = 1 period	0,1 Hz - 100 Hz, resolution 0.001 Hz
Integration time = 4 period	1 Hz - 1 kHz, resolution 0.01 Hz
Integration time = 16 period	10 Hz - 10 kHz, resolution 0.1 Hz (1 Hz)
Measuring error at the lower frequency range *	
Range 0,1 Hz - 100 Hz	< ± 0.05 %
Range 1 Hz - 1 kHz	< ± 0.05 %
Range 10 Hz - 10 kHz	< ± 0.2 %
* For Measurements in a lower frequency range, the measuring error is lower than the measuring error using the maximum frequency rang.	
Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)	
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)

Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	cULus (UL508)	
	cULus (UL1604)	Class I Div2 ABCD T4A
	DNV (Det Norske Veritas)	Cl. B
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	

More Information
Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which You can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412-0001-0101) or in the Internet under:
www.wago.com -> Service /Downloads /Documentation /WAGO-I/O-SYSTEM 750/System Description/.

2.1.4.6 Functional Description

The counter module acquires the time between one or more rising edges of the CLOCK input signal and calculates the frequency of the applied signal.

The calculation and process image update are initiated every 1st, every 4th or every 16 th rising edge depending on the integration time selected via the CONTROL byte. The first detection of a rising edge starts the cyclic period measurement and cannot provide a valid frequency value. In this case the module will send 0xFFFFFFFFH for input information. The same input value is returned when a static high or static low signal is applied to the CLOCK input.

If there are no signal changes seen at the CLOCK input, the module can be forced to update the process image after defined parameterizable time spans (Watchdog time). In this state the module will send the non valid value 0xFFFFFFFFH too.
The following figures illustrate a process data cycle.

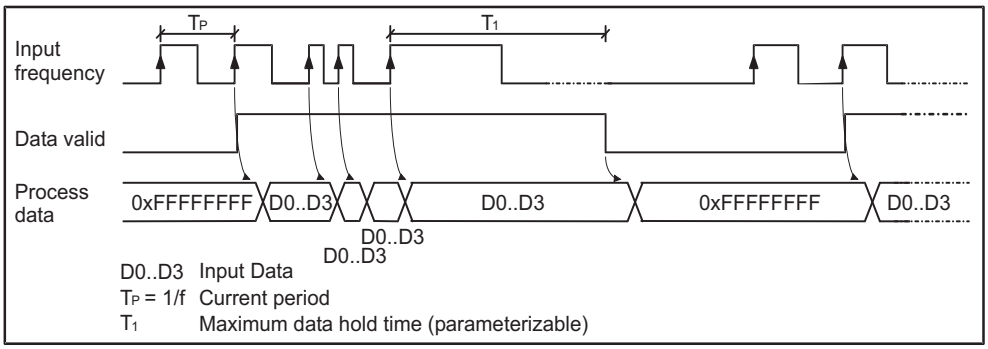

Fig. 2.1.4-4: Timing diagram for process data update sequence
(integration time = 1 period)
g040402e

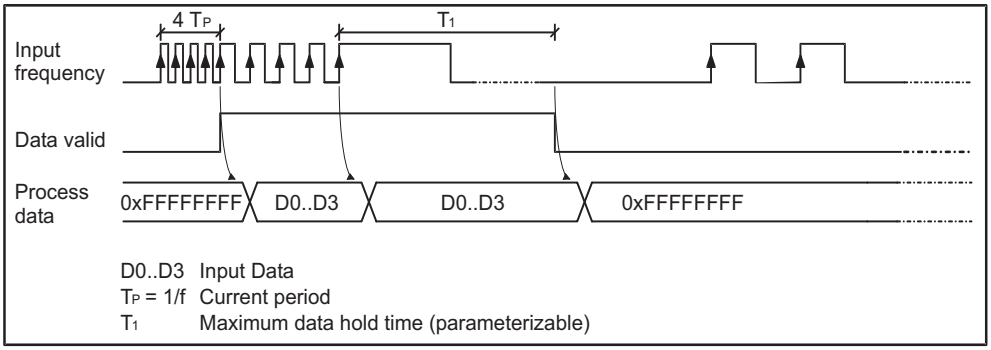

Fig. 2.1.4-5: Timing diagram for process data update sequence
(integration time = 1 period)
g040403e

2.1.4.7 Process Image

Using the I/O module 750-404/000-003, a 5 byte input and output process image can be transferred to the fieldbus coupler / controller via two logical channels.

The two output bytes (D0, D1) contain the setting Watchdog time in binary format. The other output bytes (D2, D3) are not used. The four input bytes (D0 ... D3) contain the frequency value in binary format. The control byte C0 serves for setting the integration time, the Watchdog time, the representation of the measured frequency value and the outputs. The status byte S0 displays the acknowledgement of the settings and shows the status of the inputs and outputs.

Attention
The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte	C0	Control byte
D0	Frequency value byte 0 (LSB)	D0	Watchdog-time byte 0 (LSB)
D1	Frequency value byte 1	D1	Watchdog-time byte 1 (MSB)
D2	Frequency value byte 2	D2	reserved
D3	Frequency value byte 3 (MSB)	D3	reserved

Control byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B 0**
0	0	0	T_{VD} REQ	Set output DO 2	Set output DO 1	RANGE_ SEL REQ1	RANGE_ SEL REQ0

T_{VD} REQ	Request to change the Watchdog time (T_{VD}) with valid data.
RANGE_SEL REQ1	Selection of the integration time and the representation of measured frequency value.
RANGE_SEL REQ0	Selection of the integration time and the representation of measured frequency value.
0	This constant must be set to zero.

Status byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	ST_ GATE	T_{VD} ACK	Status output DO 2	Status output DO 1	RANGE_ SEL ACK1	RANGE_ SEL ACK0

ST_GATE	Status of the GATE input (0=enabled, 1=disabled)
T_{VD} ACK	Acknowledgement T_{VD} changed.
RANGE_SEL ACK1	Acknowledgment to Range Selection, Frequency values are valid.
RANGE_SEL ACK0	Acknowledgment to Range Selection, Frequency values are valid.
X	This value is not evaluated.

With the control and status byte the following tasks are possible:

Setting the Method of Measuring, Frequency Range and Representation:
The method of measuring and the representation depends on the RANGE_SEL REQ bits in the CONTROL byte. Dependent on the adjusted measuring method also the maximum frequency range changes.
The following table illustrates the different modes.

RANGE_ SEL1	RANGE_ SEL0	Measuring method	Maximum frequency range	Measured – value display
		Integration over ...		
0	0	1 period	0.1 Hz ... 8 kHz	Frequency in 1/1000 Hz
0	1	4 periods	0.25 Hz ... 32 kHz	Frequency in 1/100 Hz
1	0	16 periods	1 Hz ... 100 kHz	Frequency in 1/10 Hz
1	1	16 periods	1 Hz ... 100 kHz	Frequency in Hz

Attention
When a new frequency range is requested, the application has to wait for valid data until the RANGE_SEL ACK bits contain the new frequency range.

The maximum delay can be calculated using the following formula:

$$T_{Dmax} = 2 \cdot \frac{\text{number of periods to be integrated}}{\text{actual frequency}}$$

If the gate is enabled the input data contains the last valid frequency value. In this state the application cannot request a new range.

Attention
If the maximum possible frequency of the different ranges is raised (see the table with maximum frequency ratings), the module will return the non valid data 0xFFFFFFFF$_H$.

Set Watchdog time:
To recognize static CLOCK signals, a watchdog timer is implemented. The standard value for the timer is 10s. The timer resets on every Power On.

The application is able to change the watchdog time during operation by using the CONTROL byte.

This can be initiated by writing the corresponding value into the output bytes D 1 and D 0 before setting the T_{VD} REQ bit in the CONTROL byte.

The success of the parameter transfer is acknowledged by the module via the T_{VD} ACK bit in the STATUS information.

Attention
The range of the watchdog timer stretches from 0 to 16383ms (0x0000 to 0x3FFF) in steps of 1ms per digit. Values which raise the permitted range of the watchdog timer are masked with 0x3FFF.

Set Outputs:
Bits 2 and 3 set the additional two outputs of the counter module.

2.1.4.8 Example

Changing the Method of Measurement, Frequency and Representation:
The frequency counter is set to a measurement range of 1 Hz ... 100 kHz with a resolution of 1/10 Hz and 16 measurement periods.

14. Set the new measurement range with the bits 0 and 1 (RANGE_SEL REQ 0 and 1) in the control byte.

Control byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	X	X	X	X	0	1

15. Wait for the feedback from the counter module in the status byte, bit 0 and 1 (RANGE_SEL ACK 1 and 0). The status byte has the following bits:

Status byte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	X	X	X	X	X	X	0	1

16. After the expiration of the delay the current frequency value with the adjusted resolution then appears in the input data with the following data bytes D0 to D3:

Data bytes				
Input data	**D3**	**D2**	**D1**	**D0**
Value	0x..	0x..	0x..	0x..

Change the Watchdog Time:
The Watchdog time is change to 5000 ms (hexadecimal value 0x1388).

17.Write the new Watchdog time value into the output bytes.
The data bytes D0 to D3 of the output data then read as follows:

Data bytes				
Output data	**D3**	**D2**	**D1**	**D0**
Value	0x00	0x00	0x13	0x88

18.With bit 4 (T_{VD} REQ) in the Control byte the changes are adopted.

Control byte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	X	1	X	X	X	X

19.After feedback of the counter module with bit 4 (T_{VD} ACK) in the status byte the counter works with the new Watchdog time.

Status byte								
Input sbit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	X	X	X	1	X	X	X	X

20.Reset bit 4 in the control byte.

Control byte								
Outout bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	X	0	X	X	X	X

21.The resetting is acknowledged with bit 4 in the status byte.

Status byte								
Input sbit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	X	X	X	0	X	X	X	X

X is used if a value is not relevant.

2.1.5 750-404/000-005 [2 Up Counter/16 Bit/5 kHz]

2 Up Counter 16 Bit, DC 24 V, 5 kHz

2.1.5.1 View

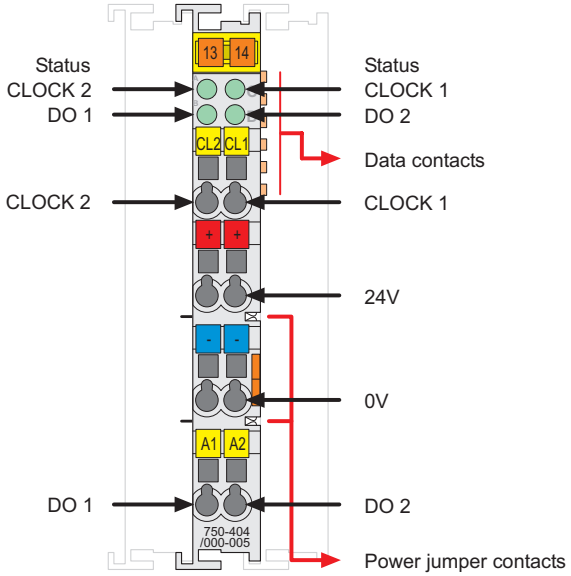

Fig. 2.1.5-1: Up Counter 750-404/000-005 g040412e

2.1.5.2 Description

The counter module also can be ordered as two Up Counters with 16 bits counter values; 750-404/000-005.
The Up counters are capable of counting binary pulses of DC 24 V at the inputs CLOCK 1 and CLOCK 2 and then transmit the data to the fieldbus. The changes from 0 V to 24 V are counted.

The counter can be set or reset with the control byte.

The digital outputs DO1 and DO2 can be activated via specific bits in the Control byte.

The outputs are short-circuit-protected.

The high states of the inputs CLOCK 1 and CLOCK 2 and the output channels are each indicated by a LED.

An optocoupler is used for electrical isolation between the bus and the field side.

Any configuration of the counter modules is possible when designing the fieldbus node. Grouping of module types is not necessary.

The field side supply voltage of 24 V for the counter module is derived from adjacent I/O modules or from a supply module. The supply voltage for the field side is made automatically through the individual I/O modules by means of power jumper contacts.

Warning
The maximum current of the internal power jumper contacts is 10 A. When configuring the system it is important not to exceed the maximum/sum current. However, if such a case should occur, another supply module must be added.

Attention
This module has no power contacts for receiving and transmitting the ground (earth) potential. A supply module is required, if the adjacent modules need to be connected to the ground.

Note
Use an appropriate supply module (e.g. 750-602) if an electrically isolated voltage supply is required!

The module 750-404/000-005 can be used with all couplers/controllers of the WAGO-I/O-SYSTEM 750 (except for the economy types 750-320, 750-323, 750-324 and 750-327 and the ModBus controllers 750-812, 750-812/025-000 and 750-814).

This description is valid for the XXXX3A05... hardware and software versions. The version is specified in the manufacturing number, which is part of the lateral marking on the module.

2.1.5.3 Display Elements

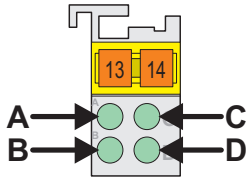

Fig. 2.1.5-2: Display Elements g041402x

LED	Channel	Meaning	State
A green	Status CLOCK 2	off	Input CLOCK 2: Signal voltage (0)
		on	Input CLOCK 2: Signal voltage (1), Counting pulse 2
B green	Status DO 1	off	Digital Output DO 1 reset
		on	Digital Output DO 1 setting
C green	Status CLOCK 1	off	Input CLOCK 1: Signalspannung (0)
		on	Input CLOCK 1: Signalspannung (1), Counting pulse 1
D green	Status DO 2	off	Digital Output DO 2 setting
		on	Digital Output DO 2 reset

2.1.5.4 Schematic Diagram

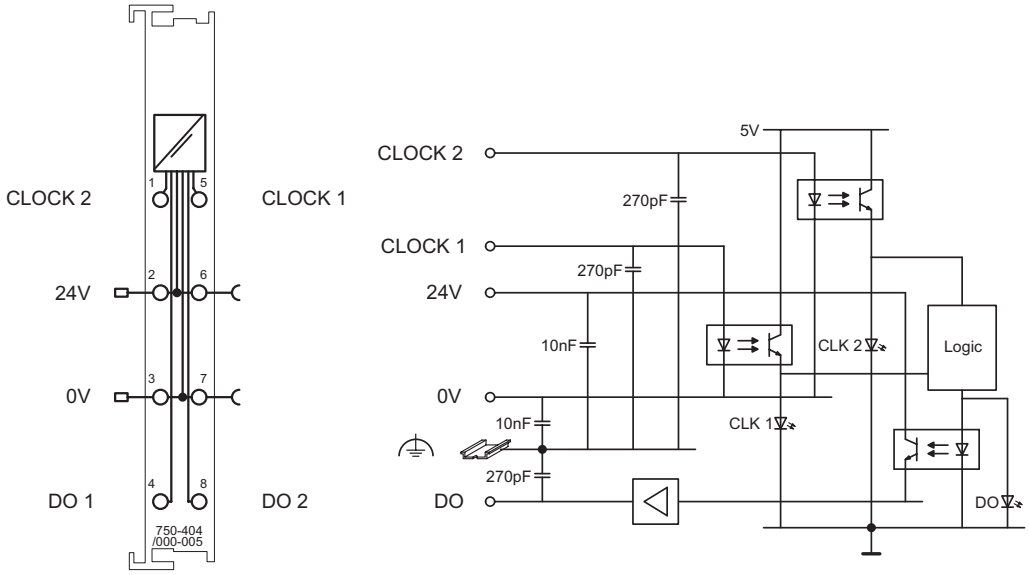

Fig. 2.1.5-3: Up Counter 750-404/000-005 g040413e

2.1.5.5 Technical Data

Module Specific Data		
Number of outputs	2	
Number of counters	2	
Output current	0.5 A short-circuit-protected	
Current consumption	75 mA	
Voltage via power jumper contacts	DC 24 V (–15 % ... + 20 %)	
Signal voltage	(0): DC –3 V ... +5 V (1): DC +15 V ... +30 V	
Switching rate $_{max.}$	5 kHz (pulse width > 100 µs)	
Input current $_{typ.}$	5 mA	
Counter depth	2 x 16 bits data	
Isolation	500 V (System/Supply)	
Internal bit width	2 x 16 bits data 8 bits control /status	
Dimensions (mm) W x H x L	12 x 64* x 100 * from upper edge of 35 DIN rail	
Weight	ca. 55 g	
Standards and Regulations (cf. Chapter 2.2 of the Coupler/Controller Manual)		
EMC-Immunity to interference (CE)	acc. to EN 50082-2 (96)	
EMC-Emission of interference (CE)	acc. to EN 50081-1 (93)	
Approvals (cf. Chapter 2.2 of the Coupler/Controller Manual)		
	$_{C}UL_{US}$ (UL508)	
	$_{C}UL_{US}$ (UL1604)	Class I Div2 ABCD T4A
	DNV (Det Norske Veritas)	Cl. B
	KEMA	II 3 G EEx nA II T4
	Conformity Marking	

More Information
Detailed references to the approvals are listed in the document "Overview Approvals WAGO-I/O-SYSTEM 750", which You can find on the CD ROM ELECTRONICC Tools and Docs (Item-No.: 0888-0412-0001-0101) or in the Internet under:
www.wago.com -> Service /Downloads /Documentation /WAGO-I/O-SYSTEM 750/System Description/.

2.1.5.6 Process Image

Using the I/O module 750-404/000-005, a 5 byte input and output process image can be transferred to the fieldbus coupler / controller via two logical channels.

The transfer of the setting counter values in binary format is made via 4 output bytes (D0, D1) or (D2, D3) and the transfer of the counter reading in binary format is made via 4 input bytes (D0, D1) or (D2, D3). The control byte C0 serves for setting and locking the counters and for setting the outputs. The status byte S0 shows the status of the counters and the inputs and outputs.

Attention
The representation of the process data of some I/O modules or their variations in the process image depends on the fieldbus coupler/-controller used. Please take this information as well as the particular design of the respective control/status bytes from the section "Fieldbus Specific Design of the Process Data" included in the description concerning the process image of the corresponding coupler/controller.

Input data		Output data	
S0	Status byte	C0	Control byte
D0	Counter value 1 byte 0 (LSB)	D0	Set value 1 byte 0 (LSB)
D1	Counter value 1 byte 1 (MSB)	D1	Set value 1 byte 1 (MSB)
D2	Counter value 2 byte 0 (LSB)	D2	Set value 2 byte 0 (LSB)
D3	Counter value 2 byte 1 (MSB)	D3	Set value 2 byte 1 (MSB)

Control byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
0	0	Set counter 1	Set counter 2	Set output DO 2	Set output DO 1	0	0

0 This constant must be set to zero.

Status byte							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	Counter is set	Counter is set	actual signal at output DO 2	actual signal at output DO 1	actual signal at input CLOCK 2	actual signal at input CLOCK 1

X his value is not evaluated.

With the control and status byte the following tasks are possible:

Set Counter:
Put Bit 5 (4) into the control byte. The counter 1 (2) with the 16 bit value is loaded into output bytes 0 (1) or 2 (3). As long as the bit is set, the counter can stop and information is stored. The ensuing data of the counter will be conveyed to the status byte. Bit 5 (4) in the status byte communicates the successful load of the counter.

Set Outputs:
Bits 2 and 3 set the additional two outputs of the counter module.

2.1.5.7 Example

Set Counter 1:
First of all the counter reading is set to 100 by "Setting counter", i. e. to the hexadecimal value: 0x64.

22. Enter the set value in the output data.
    The data bytes D0 to D3 of the output data then read as follows:

Datenbytes				
Output data	**D3**	**D2**	**D1**	**D0**
Value	0x00	0x00	0x00	0x64

23. Validate the counter reading in the control byte with bit 5 (setting counter 1) to have it adopted as an output value. The control byte has the following bits:

Steuerbyte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	1	X	X	X	X	X

24. Wait for the feedback from the counter module in the status byte, bit 5 (counter 1 set). The status byte has the following bits:

Statusbyte								
Input bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	X	X	1	X	X	X	X	X

25. Delete bit 5 (setting counter 1) in the control byte in order to finish the Handshake. The bits in the control byte read as follows:

Steuerbyte								
Output bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Value	0	X	0	X	X	X	X	X

26. The set counter reading then appears in the input data with the following data bytes D0 to D3:

Data bytes				
Input data	**D3**	**D2**	**D1**	**D0**
Value	0x00	0x00	0x00	0x64

27. Wait for the first and further count pulses.
During counting, the data bytes D0 to D3 of the input data appear as follows:

	Data bytes			
Remark	**D3**	**D2**	**D1**	**D0**
no count pulse received	0x00	0x00	0x00	0x64
1st count pulse received	0x00	0x00	0x00	0x65
2nd count pulse received	0x00	0x00	0x00	0x66
Further count pulses	.....	.....	.....	.....
Max. counter reading reached	0x00	0x00	0xFF	0xFF
the next count pulse causes a number overflow	0x00	0x00	0x00	0x00
One further count pulse received	0x00	0x00	0x00	0x01

X is used if a value is not relevant.

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